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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/687,252 | 10/16/2003 | Gerald Francis McBrearty | AUS920030733US1 | 9424 |

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| EXAMINER | |
|---|---|
| BAKER, PAUL A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2188 | |

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/687,252 | MCBREARTY ET AL. | |
| | Examiner | Art Unit | |
| | Paul A. Baker | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,8,9,13 and 15-20* is/are rejected.

7)☒ Claim(s) *3-5,7,10-12,14 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,6,8,9,13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bealkowski et al US Patent 6,295,591 in view of Badovinatz et al. 5,392,415 in further view of FOLDOC's definition of swap file.

In regards to claim 1, Bealkowski discloses a method memory block removal from a data processing system, comprising:

receiving a request to physically remove a memory block device from said data processing system in figure 3 element 46;

translating a plurality of logical pages for said memory block device into a plurality of physical addresses for said memory block device in figure 3 element 48; and

such that after said request is complete said memory block device can be removed in claim 3.

Bealkowski does not disclose issuing a single request to page out data located at said plurality of physical addresses to a contiguous paging space within a disk space accessible to said data processing system.

Badovinatz discloses issuing a single request to page out data located at said plurality of physical addresses to a paging space within a disk space accessible to said data processing system in column 3 lines 5-6.

Badovinatz discloses that an efficient implementation of a virtual storage system consists of efficient utilization of physical memory and efficient input/output operations (by moving as much data as possible between physical memory and auxiliary storage in a time period). Badovinatz coalesces multiple virtual memory pages into categories (examples provided are by thread and by object) and enabling the transfer of a category of pages in a single page out operation to improve the second criteria without sacrificing the first criteria. Bealkowski pages out many pages at once in Figure 3 element 48, therefore it would have been obvious to one of ordinary skill in the art to incorporate Badovinatz's method of paging out using a single operation within Bealkowski's invention.

Neither Bealkowski nor Badovinatz discloses the paging space is contiguous, both Bealkowski and Badovinatz disclose paging out physical memory to the swap file of the system, FOLDOC discloses that swap files are usually allocated as a contiguous section of a hard disk to reduce access time. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the paging space contiguous.

In regards to claim 2, Badovinatz discloses mapping said plurality of logical pages for said memory block to a plurality of physical pages for said memory block device in figure 5 element 530.

In regards to claim 6, Bealkowski discloses detecting a replacement memory block device in figure 3 element 50;

Badovinatz discloses pretranslating a plurality of logical pages for said contiguous paging space into a plurality of physical addresses for said contiguous paging space in column 5 lines 33-35; and

discloses issuing a single request to page in data located at said plurality of physical addresses to said replacement memory block device in column 5 lines 35-37, such that only two input/output requests are required for large memory block replacement.

In regards to claim 8, Bealkowski discloses a data processing system comprising:

an operating system in column 3 lines 4-7;

a processor that executes instructions of said operating system in figure 1 elements 12a;

a memory comprising a plurality of memory blocks interconnected to said processor in figure 1 element 16;

a disk space accessible to said processor in figure 2 element 38;

means for enabling removal of a particular memory block from among said plurality of memory blocks by:

translating a plurality of logical pages for said particular memory block into a plurality of physical addresses for said particular memory block in figure 3 element 48; and

Bealkowski discloses after request is complete safe removal of said particular memory block is enabled in figure 3 element 50.

Bealkowski does not disclose issuing a single request to page out data located at said plurality of physical addresses to a contiguous paging space within said disk space.

Badovinatz discloses issuing a single request to page out data located at said plurality of physical addresses to a paging space within said disk space in column 3 lines 5-6.

Badovinatz discloses that an efficient implementation of a virtual storage system consists of efficient utilization of physical memory and efficient input/output operations (by moving as much data as possible between physical memory and auxiliary storage in a time period). Badovinatz coalesces multiple virtual memory pages into categories (examples provided are by thread and by object) and enabling the transfer of a category of pages in a single page out operation to improve the second criteria without sacrificing the first criteria. Bealkowski pages out many pages at once in Figure 3 element 48, therefore it would have been obvious to one of ordinary skill in the art to incorporate Badovinatz's method of paging out using a single operation within Bealkowski's invention.

Neither Bealkowski nor Badovinatz discloses the paging space is contiguous, both Bealkowski and Badovinatz disclose paging out physical memory to the swap file of the system, FOLDOC discloses that swap files are usually allocated as a contiguous section of a hard disk to reduce access time. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the paging space contiguous.

In regards to claim 9, Badovinatz discloses means for mapping said plurality of logical pages for said memory block to a plurality of physical pages for said particular memory block in figure 5 element 530.

In regards to claim 13, Bealkowski discloses means for detecting a replacement memory block in column 5 lines 33-35;

Badovinatz discloses means for translating a plurality of logical pages for said contiguous paging space into a plurality of physical addresses for said contiguous paging space in column 5 lines 33-35; and

means for issuing a single request to page in data located at said plurality of physical addresses to said replacement memory block in column 5 lines 35-37.

In regards to claim 15, Bealkowski discloses a computer program product for selectively displaying mirrored addresses in a communication, comprising:

a computer readable medium in figure 1 element 18; and

program instructions on said computer readable medium for:

receiving a request to physically remove a memory block device from said data processing system in figure 3 element 46;

translating a plurality of logical pages for said memory block device into a plurality of physical addresses for said memory block device in figure 3 element 48;

Bealkowski discloses after request is complete said memory block can be removed in figure 3 element 50.

Bealkowski does not disclose issuing a single request to page out data located at said plurality of physical addresses to a contiguous paging space within a disk space accessible to said data processing system.

Badovinatz discloses issuing a single request to page out data located at said plurality of physical addresses to a paging space within a disk space accessible to said data processing system space in column 3 lines 5-6.

Badovinatz discloses that an efficient implementation of a virtual storage system consists of efficient utilization of physical memory and efficient input/output operations (by moving as much data as possible between physical memory and auxiliary storage in a time period). Badovinatz coalesces multiple virtual memory pages into categories (examples provided are by thread and by object) and enabling the transfer of a category of pages in a single page out operation to improve the second criteria without sacrificing the first criteria. Bealkowski pages out many pages at once in Figure 3 element 48, therefore it would have been obvious to one of ordinary skill in the art to incorporate

Badovinatz's method of paging out using a single operation within Bealkowski's invention.

Neither Bealkowski nor Badovinatz discloses the paging space is contiguous, both Bealkowski and Badovinatz disclose paging out physical memory to the swap file of the system, FOLDOC discloses that swap files are usually allocated as a contiguous section of a hard disk to reduce access time. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the paging space contiguous.

In regards to claim 16, Badovinatz discloses means for mapping said plurality of logical pages for said memory block to a plurality of physical pages for said particular memory block in figure 5 element 530.

In regards to claim 20, Bealkowski discloses means for detecting a replacement memory block in column 5 lines 33-35;

Badovinatz discloses translating a plurality of logical pages for said contiguous paging space into a plurality of physical addresses for said contiguous paging space in column 5 lines 33-35; and

issuing a single request to page in data located at said plurality of physical addresses to said replacement memory block device in column 5 lines 35-37.

***Allowable Subject Matter***

Claims 3-5, 7, 10-12, 14, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan
10/28/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER